to a subscriber through a tip terminal and a ring terminal;

a second [pair of transistors (Q3, Q4)] third transistor and a fourth transistor having a Darlington structure, [and] connected to said first and second transistors [(Q1, Q2)] respectively, and limiting a maximum current;

a first pair of current supervising resistors [(R1, R2)] respectively connected to emitters of said first [pair of] and second transistors [(Q1, Q2) respectively] for, performing a current feedback operation to limit said maximum current[,] and for detecting [in] a voltage [form] from a line current flowing through telephone lines;

a first resistor [(R3)] connected between a collector of one of said first [pair of transistors (Q1)] transistor and a collector of [one of] said [second] third transistor [(Q3)], preventing [one of] said first [pair of transistors (Q1)] transistor from being saturated;

a second resistor [(R4)] connected between a collector of [the other one of] said second [transistors (Q2)] transistor and a collector of [the other one of] said [second pair of transistors (Q4)] fourth transistor, preventing said second transistor [(Q2)] from being saturated;

a [group] plurality of bias resistors [(R5, R6, R7)] for determining a threshold value of said maximum current and [maintaining] allowing said first [pair of] and second transistors [(Q1, Q2)] in an active state;

a [first] pair of first capacitors [(C5, C6)] superimposing a received [AC audio] signal on a DC line current;

a pair of composite impedances [(ZL1, ZL2)] for matching a line characteristic impedance;

a third resistor [(R11)] for converting said line current flowing through a first one of [the]

said current supervising resistors [(R1)] into an input current for detecting an off-hook state;

an operational amplifier [(AMP3)] inversion-amplifying a signal inputted through said third resistor [(R11)]; and

a fourth transistor [(Q6)] converting a level of a signal inversion-amplified by said operational amplifier.

2. (Amended) The [analog subscriber matching] interface circuit of claim 1, further comprising a pair of amplifiers [(AMP1, AMP2)] connected to said composite impedances [(ZL1, ZL2)], respectively, for receiving and amplifying the audio signal.

3. (Amended) The [analog subscriber matching] interface circuit of claim 2, further comprising a pair of protection elements [(CR1, CR2)] for protecting said amplifiers for amplifying said audio signal from an over current through lines.

4. (Amended) The [analog subscriber matching] interface circuit of claim 3, further comprising a dummy load resistor [(R8)] connected between the collector of [one of] said first [pair of transistors (Q1)] transistor and the collector of [the other one of] said [first pair of transistors (Q2)] second transistor for supplying a bias current to said first [pair of ] and second transistors (Q1, Q2) to prevent said first [pair of] and second transistors [(Q1, Q2)]from being saturated when no load exists on said line.

5. (Amended) The [analog subscriber matching] interface circuit of claim 4, further comprising a pair of temperature compensating diodes [(D1, D2)] connected to opposite sides of said plurality of bias [resistor group (R5, R6)] registors, respectively, for preventing said first [pair of] and second transistors [(Q1, Q2)] from being overheated due to a variation of the threshold value of said maximum current caused by the heat generated from said first [pair of] and second transistors [(Q1, Q2)] due to the line current.

6. (Amended) The [analog subscriber matching] interface circuit of claim 5, further comprising a plurality of bypass capacitors [(C1, C2, C3)] preventing a bad influence on call communications due to the generation or induction of noise in said DC line current supply.

7. (Amended) The [analog subscriber matching] interface circuit of claim 6, further comprising a fifth resistor [(R13)] for determining an amplification factor of said signal inputted through said third resistor [(R11)].

8. (Amended) The [analog subscriber matching] interface circuit of claim 7, further comprising a sixth resistor [(R10)] for detecting a ring trip voltage if a telephone handset is hooked off during supply of a call signal.

9. (Amended) The [analog subscriber matching] interface circuit of claim 8, further comprising a seventh resistor [(R12)] converting the voltage detected by said sixth resistor [(R10)]

into a ring trip current.

10. (Amended) The [analog subscriber matching] interface circuit of claim 9, further comprising a second capacitor [(C7)] allowing said operational amplifier [(AMP3)] to serve as a low-pass filter so that an AC amplification factor is greatly lowered to remove AC ripple components included in said ring trip current.

11. (Amended) The [analog subscriber matching] interface circuit of claim 10, further comprising a field effect transistor [(FET1)] allowing said operational amplifier [(AMP3)] to serve as a low-pass filter in a ring current supply state.

--12. A subscriber line interface circuit, comprising,

a first terminal having a first reference voltage;

a second terminal having a second reference voltage;

a first voice line; and

a first current limiting circuit connected between said first terminal and said first voice line, including:

a first transistor a having an emitter, a collector connected to said first voice line, and a base;

a first current supervising register connected between said emitter of said first transistor and said first terminal;

a second transistor having an emitter connected to said base of said first transistor, a collector, and a base;

a second register connected between said collectors of said first and said second transistor;

a third register connected between said base of said second transistor and said first terminal; and

a fourth register connected between said base of said second transistor and said second terminal.

--13. The subscriber line interface circuit of claim 12, further comprised of:

a second line: and

a second current limiting circuit connected between said second terminal and said fourth transistor, including:

a third transistor a having an emitter, a collector connected to a second line, and a base;

a second current supervising register connected between said emitter of said first transistor and said second terminal;

a fourth transistor having an emitter connected to said base of said third transistor, a collector, and a base;

a fifth register connected between said collectors of said third and fourth transistor; and

a sixth register connected between said base of said second transistor and said second terminal.

--14. The subscriber line interface circuit of claim 13, further comprised of said a dummy register coupled between said first line and said second line.

--15. The subscriber line interface circuit of claim 12, further comprised of a first capacitor connected between said base of said first transistor and said first terminal.

--16. The subscriber line interface circuit of claim 12, further comprised of a second capacitor connected between said base of said second transistor and said first terminal.

--17. The subscriber line interface circuit of claim 13, further comprised of a third capacitor connected between said base of said third transistor and said second terminal.

--18. The subscriber line interface circuit of claim 13, further comprised of a fourth capacitor connected between said base of said fourth transistor and said second terminal.

--19. The subscriber line interface circuit of claim 13, further comprised of:

an seventh register;

an operational amplifier connected to said emitter of said first transistor and said first

reference terminal through a eighth register; and

a switch connecting said seventh register to said amplifier and said eighth register during an off hook state.

--20. The subscriber line interface circuit of claim 13, further comprised of:

a first pair of temperature compensating diodes connected between said first terminal and said base of said second transistor; and

a second pair of temperature compensating diodes connected between said second terminal and said base of said fourth transistor.